WHAT IS CLAIMED IS:

1. A processor, comprising:

a processor core; and

a memory operatively coupled to said processor;

wherein said processor is designed using the method comprising:

selecting a cache size;

selecting an instruction memory size;

selecting a data memory size;

selecting at least one of a plurality of option instructions to be implemented within said processor core.

2. The processor according to Claim 1, wherein said option instructions include a dividing option instruction (DIV) and a maximum/minimum value option instruction (MINMAX).

3. The processor according to Claim 1, wherein said processor core is provided with an instruction cache and a data cache.

4. The processor according to Claim 1, wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates.

5. The processor according to Claim 1, wherein said method further comprises selecting optional hardware associated with said processor.

6. A system LSI, comprising:

a processor core;

a memory operatively coupled to said processor and a user defined module; wherein said processor is configured using the method comprising:

selecting a cache size;

selecting an instruction memory size;

selecting a data memory size;

selecting at least one of a plurality of option instructions to be implemented within said processor.

7. The system LSI according to Claim 6, wherein said option instructions include a dividing option instruction and a maximum/minimum value option instruction.

8. The system LSI according to Claim 6, wherein said processor is provided with an instruction cache and a data cache.

9. The system LSI according to Claim 6, wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates.

10. A method of generating a design of a system LSI using a description language, comprising:

preparing a configuration specifying a file including variable item definition information;

logically composing said design based on said description language model, wherein said variable item definition information contains at least one item of option instruction information and information concerning a user defined module and a multiprocessor configuration.

11. The method of Claim 10, wherein said description language comprises a hardware description language (HDL).